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EXAMINER	
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ART UNIT	PAPER NUMBER
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NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/673,467	STRANG, ERIC J.	
	Examiner	Art Unit	
	AKASH SAXENA	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-61 has/have been presented for examination based on amendment filed on 19th February 2008.
2. Claim(s) 1, 28, 55 and 58 is/are amended.
3. Claim(s) 1-61 remain rejected under 35 USC § 112 with addition of new basis of rejection.
4. Claim(s) 1-61 remain rejected under 35 USC § 103.
5. The arguments submitted by the applicant have been fully considered. Claims 1-61 remain rejected and this action is made **FINAL**. The examiner's response is as follows.

Response the applicant's remarks for Claim Rejections - 35 USC § 101

6. Examiner withdraws the claim rejection(s) under 35 USC § 101 to claim(s) 58 in view of the applicant's amendment exclusively citing volatile media and non-volatile media from disclosure on page 33 of the specification.

Response to Double Patenting

7. Applicant's arguments relating to filing a terminal disclaimer for applications 10/673,507, *10/673,501, 10/673,138, 10/673,583 (Added)* are considered and double patenting rejection is maintained until a terminal disclaimer is filed.

Response the applicant's remarks for Rejections under- 35 USC § 112¶1st

8. Applicant has provided an exact support in disclosure for such attributes in the model. Applicant has quoted specification paragraphs [0035] and [0036] in support. These paragraph are not enabling although they rely on the commercially available packages to model the various first principle simulation models, **the details of the model are absent from the specification.** The details of these model which lead to **unexpected results without under experimentation** are very relevant to the designing the first principle physical model.

   Specification ¶ [0035] states:

   > First principles physical model 106 is a model of the physical attributes of the tool and tool environment as well as the fundamental equations necessary to perform first principles simulation and provide a simulation result for facilitating a process performed by the semiconductor processing tool. **Thus, the first principles physical model 106 depends to some extent on the type of semiconductor processing tool 102 analyzed as well as the process performed in the tool.** For example, the physical model 106 may include a….

   No where in the disclosure are details of any model presented to enable the first principal model for any tool. Further applicant has not presented any citation that this is known in the art. Merely stating that one tools first principal model different from another (see [0035] for statement regarding CVD tool model different from diffusion furnace tool model) does not teach the model itself.

9. Further regarding claims 6-9, (Remarks Pg. 18), applicant argues inputting data and computer codes – none of which appears to be presented in the specification and applicant has failed to specifically cite relevant section of the specification. Hence the argument is unpersuasive.

10. Further regarding Remarks Pg. 19 for **unexpected results**, direct attention to claims 15-19. These claims merely state that execution of first principle model can be performed in networked facilities. Enhancement in real time simulation due to this networking is not unexpected result (See Jain Section IV & V). Further this does not obviate what constitutes a first principle model and how it is faster than other known methods of simulation (at least see Sonderman: at least in Col.5 Lines 11-17; 49-67).

11. Further regarding Remarks Pg. 19, applicant states:

> Below are Claims 15-19 and 59 reproduced for the examiner's convenience showing the networking of interconnected resources inside a semiconductor device manufacturing facility, the sharing of computational load, and the distribution of similar simulation results (for example as initial boundary conditions) to reduce redundant refinements and execution and permit a first principles simulation result to be produced in a time frame shorter in time than the actual process being performed:

This is a conclusory statement, without *rationale* and *support* from specification.

Examiner respectfully maintains the rejection.

Response to Applicant's Remarks for 35 U.S.C. § 103

12. **Claims 1-21, 23, 25-48, 50 and 52-58 were rejected under 35 U.S.C. 103(a) as being unpatentable over Sonderman, in view of Chen, further in view of Jain.**

Regarding Claims 1-21, 23, 25-48, 50 and 52-58

(Argument 1) Applicant has argued in Remarks Pg.21:

> The plain reading of this section of Sonderman et al is that the system 100 then (e.g., at time T1) optimizes the simulation for each silicon wafer, Si to be processed (e.g., later at time T2). In other words, the simulation results of Sonderman et al produce a new control input for each silicon **wafer to be processed**. Thus, Applicant respectfully submits that Sonderman et al teach performing first principles simulation for the actual process to be performed before performance of the actual process, and **not** the claimed performing first principles simulation for the actual process being performed during performance of the actual process.

(Response 1) Examiner disagrees with applicant's interpretation as applicant is misreading the disclosure. Wafers to be processed may be wafers which are awaiting processing pending simulation result or alternately, in process still waiting alteration to process based on the process data. Applicant has not cited the complete paragraph (Sonderman: Col.9 Lines 42-51)

> The system 100 then optimizes the simulation (described above) to find more optimal process target (T.sub.i) for each silicon wafer, S.sub.i. to be processed. These target values are then used to generate new control inputs, X.sub.Ti, on the line 805 to control a subsequent process of a silicon wafer S.sub.i. The new control inputs, X.sub.Ti, are generally based upon a plurality of factors, such as simulation data, output requirements, product performance requirements, process recipe settings based on a plurality of processing tool 120 operating scenarios, and the like.

Essentially, applicant is arguing granularity of the process described in Fig.4 and Fig.1, whereas no such indication, for or against, is present in Sonderman. Hence applicant is reading their specification into Sonderman for teaching away. Fig.1 shows a feedback cycle where actual process is using simulation data. Examiner thanks applicant for the remarks above, however the new control inputs are not developed for the processing of each subsequent wafer, but instead are for

subsequent processing [performed on] a silicon wafer S.sub.i (Sonderman: Col.9 Lines 44-46 – this point is also addressed above in response to argument 1).

Further ***most importantly*** applicant is arguing limitation, which are not present in the claim and may constitute patentable subject matter. Specifically, as indicated by applicant "the lengthy time for generation of a first principles model simulation in the prior art prevents one from realizing a real time process control based on a first principles simulation during the actual process." However, this is the conclusory statement, where what makes the current first principle simulation model realize the real time process control possible is not claimed. Further distinguishing it from Sonderman may also help in defining a more patentable subject matter.

Examiner respectfully maintains the rejection and finds the argument unpersuasive.

(Argument 2) Applicant has argued in Remarks Pg.23:

Chen and Sonderman do not teach the newly amended limitation of "shorter time frame" in the independent claims.

(Response 2) Chen and Sonderman are not used for this rejection. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Jain is used to address this limitation (See rejection below).

(Argument 3) Applicant has argued in Remarks Pg.24:

Applicant has argued disclosure of Jain requires futuristic computational equipment.

(Response 3) Networked computing is well known in the art at the time of invention and Section IV and V of Jain disclose various forms of networked computing. These are not futuristic equipments. Further applicant's own disclosure is scant on the argued limitation.

Arguments pertaining to Kee et al are moot as Kee et al not used in the rejection.

(Argument 4) Applicant has argued in Remarks Pg.27:

Arguments pertaining to Sonderman alone, with reference decision rendered in KSR International Co. v. Teleflex Inc. et al, applicant has argued that unexpected results.

(Response 4) Applicant's allegations are not supported by specification showing unexpected results; instead applicant is performing piecemeal analysis using a single reference. Sonderman does no teach away alleged by applicant. Jain teaches real time for generation of first principle model simulation (through MPE engine) (Jain Abstract). Examiner disagrees that there are any unexpected results.

Claim Rejections - 35 USC § 112¶1st

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

13. Claim 1-61 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. *Exact details of what basic physical and chemical attribute of the semiconductor processing tool are used to construct a first principle simulation model* which is critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Secondly, applicant has amended limitation:

> said first principles simulation result being produced <u>in a time frame shorter in time than the actual process being performed</u>;

There is no support cited in the specification for this limitation. Arguendo even if cited the statement itself does enable how the first principle simulation results are produced in the time from shorter in time than the actual process. Due to lack of the details of the model this determination can further cannot be made.

Applicant has argued citing specification paragraphs [0035] and [0036] as to what constitutes first principle physical model. None of which support the above two basis of the rejection.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

14. Claim 1, 26, 55 and 56 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1, 38, 75 and 78 of copending Application No. 10/673,507 (updated 9/19/06) respectively.

Application No. 10/673,467	Application No. 10/673,507
A method of controlling a process performed by a semiconductor processing tool, comprising:	A method of controlling a process performed by a semiconductor processing tool, comprising:
inputting data relating to a process performed by the semiconductor processing tool;	inputting data relating to a process performed by the semiconductor processing tool;
inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attributes of the semiconductor processing tool;	inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool;;
performing first principles simulation *for the actual process being performed* **using the input data** and the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being	performing first principles simulation *for the actual process being performed* using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed; and

performed;	
using the first principles simulation result to build an empirical model; and	
selecting at least one of the first principles simulation result and the empirical model to control the process performed by the semiconductor processing tool.	and using the first principles simulation result to control the *actual* process performed by the semiconductor processing tool.

Although the conflicting claims are not identical, they are not patentably distinct from each other because the step of building an empirical model is inherent with the physical model. Further, both the specifications are identical in implementation and there is no difference in the implementation of the two models. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented. Further the step of "selecting" which not present in the 10/673,507, is evident in the using the result to control the actual process.

15. **Further, at least Claim 1 is also provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/673,501, 10/673,138, 10/673,583.** The steps of controlling, inputting data, inputting a first principle physical model, performing simulation and selecting/using results are almost identical in the both the claim 1 sets for the co-pending applications. Other independent claims in the copending applications are rejectable similarly.

---------- End of Double Patenting Rejection ----------

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

16. Claims 1-21, 23, 25-48, 50 and 52-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter).

Regarding Claim 1 (Updated 5/21/08)

Sonderman teaches a method to controlling a process performed by a semiconductor-processing tool (Sonderman: Summary, at least in Col.2 Lines 10-17;Col.3 Lines 45-49) by inputting *process* data relating to *an actual* process *being* performed by the semiconductor-processing tool (Sonderman: at least in Col.3 Lines

50-67; *Col.7 Lines 8-20*). Further, Sonderman teaches inputting the first principle physical model relating to the semiconductor-processing tool *describing at least one of a basic physical or chemical attributes* (Sonderman: at least in Col.5 Lines 11-17; 49-67) as device physics model, a process model and an equipment model. Further, Sonderman teaches performing first principle simulation *for the actual process being performed* during performance of actual process *(Sonderman: Col.7 Lines 4-7; Col.3 Lines 56-63; Fig. 1-3)* using the input data and the physical model to provide simulation results for the process performed by the semiconductor–processing tool (Sonderman: at least in Col.5-7). Further, Sonderman teaches using the first principle simulation results obtained *during the performance of the actual process* (Sonderman: Fig. 1-3 *Col.7 Lines 4-7; Col.3 Lines 56-63*) to control the *actual* process *being* performed by the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 48-64; Fig.1-8; Col.2 Lines 10-17).

Sonderman does not explicitly teach building an empirical model and using the first principle simulation results along with the empirical model to control the process performed by the semiconductor-processing tool. Empirical model & library as understood from the specification ([0078]) is the database of the simulation results, which provides "statistically sufficient sample of the parameter space".

Chen teaches creating an empirical model as disclosed in the specification as a statistical model built based on run-to-run or batch-to-batch results and using the results to control the process performed by the semiconductor-processing tool as well as to the next simulation step (Chen: Col.3 Lines 12-47; Col.6 Lines 34-67).

Sonderman and Chen do not teach first principle model including a set of computer encoded differential equations.

Jain teaches computer encoded differential equations using MPE engine, which can be applied to wafer processing (Jain: Abstract). Jain also teaches dedicated and wafer level implementation of MPE engine to provide enhanced performance (Jain: Pg. 372 Section V Dedicated MPE).

Jain also teaches said first principles simulation (MPE Engine) result being produced in a time frame shorter in time than the actual process being performed as MPE engine solving the problem in real time (Jain: Abstract), with further speed-up possible by distributed simulation and enhancement in wafer technology (Jain: Fig.4 & 5 and sections IV and V).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Chen to Sonderman. The motivation to combine would have been that Chen and Sonderman both are analogous art concerned with simulating the semiconductor fabrication process and providing the best control parameters to the actual semiconductor-processing tool (Chen: at least in Col.3 Lines 19-23).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Jain to Sonderman to solve differential equation for the semiconductor processing tool. Sonderman teaches building various models, which work in real-time feedback control simulating actual semiconductor modeling process (Sonderman: Fig.1; *Col.7 Lines 8-20*), while

Jain makes possible by providing model-solving capacity in real time when differential equations are present in the model (like thermal patterns in semiconductor wafer model) (Jain: Abstract).

Regarding Claim 2

Sonderman teaches directly inputting the *process* data relating to the *actual* process *being* performed by the semiconductor-processing tool from at least one of physical sensor (eg. Scatterometry data, overlay data, dimensional data) and a metrology tool physically mounted on the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 31-48; Col.4-8; Fig.1, 7; *Col.7 Lines 8-20*).

Regarding Claims 3-5

Sonderman teaches indirectly inputting the *process* data relating to the *actual* process performed by the semiconductor-processing tool from one of the manual input devices and a database as manual fashion data retrieval and automatic data retrieval; inputting data recorded from the previous run; inputting the data set by a simulation operator (Sonderman: at least in Fig.1-3 Col.1; Col.4-7; Col.7 Lines 8-20).

Regarding Claims 6-9

Sonderman teaches inputting *process* data relating to at least one of the physical characteristics of the semiconductor-processing tool and semiconductor tool environment, data relating to at east on of the characteristics and a result of a process performed by the semiconductor processing tool; inputting a spatially resolved model (as modified models) of the geometry of the semiconductor processing tool; inputting fundamental equations necessary to perform first principle

simulation for the desired simulation result (Sonderman: at least in Col.5 Lines 10-18; Col.6 Lines 48-63; Col.9 (equations); Col.5-9; Fig 1-3; *Col.7 Lines 8-20*). Sonderman and Jain teach inputting fundamental equations *as the set of computer encoded differential equations* (Sonderman: Col.9 (equations); Jain: Pg. 372 Section V Dedicated MPE, Abstract).

Regarding Claim 10

Sonderman teaches performing interaction concurrently between the simulation environment (first principle simulation) and the semiconductor-processing tool (Sonderman: Fig.2; Col.4 Lines 48-63).

Regarding Claims 11-13

Sonderman teaches performing first principle simulation independent of the process performed by the semiconductor-processing tool; inputting data from to set initial & boundary condition on the first simulation model (Sonderman: at least in Col.5-8; Fig.3-4).

Regarding Claim 14

Sonderman teaches using the first principles simulation result comprises using the first principles simulation result to perform at least one of detecting, and classifying a fault in the process performed by the semiconductor-processing tool (Sonderman: at least in Col.5 Line 56 – Col.6 Line 24).

Regarding Claims 15-19

Sonderman teaches using a network of interconnected resources inside the semiconductor manufacturing facility (Sonderman: Semiconductor tools on the

factory floor – Col.9 Lines 60-65) to perform first principle simulation (Jain: Section III) recited in claim 1; using code parallelization among interconnected computational resources to share the computational load of the first principle simulation; sharing simulation information among the interconnected resources to facilitate a process by the semiconductor-processing tool; sharing simulation results among the interconnected resources to reduce redundant execution of substantially similar first principle simulation by different resources; sharing information comprising model changes among the interconnected resources to reduce the redundant refinements of first simulation by different resources (Sonderman: Fig.1-3, computer code software is described in Col.9 Lines 58 onward; Col.5-8).

Regarding Claims 20-21

Sonderman teaches remote access to computational and storage resources (Sonderman: Col.9 Line 58-Col.10 Line 31) where in wide area network is art inherent.

Regarding Claim 23

Sonderman teaches first principle simulation controlling at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace (Sonderman: at least in Col 4 Lines 18-31; Col.3 Lines 45-49).

Regarding Claim 25

Sonderman teaches inputting various parameters relating to etching, deposition etc. (Sonderman: at least in Col.5 Lines 56-67)

Regarding Claim 26

Sonderman teaches inputting physical geometric data as parameters for the equipment model where the equipment could be at least one of a material processing system, an etch system, a photoresist spin coating system, a lithography system, a dielectric coating system, a deposition system, a rapid thermal processing system for thermal annealing, and a batch diffusion furnace (Sonderman: Col.5 Lines 56-67).

Regarding Claim 27

Sonderman teaches first principles simulation result controlling the semiconductor processing tool by using model output to adjust said process performed by the semiconductor processing tool (Sonderman: Col.4 Lines 48-64; Fig.1-2).

Regarding Claim 28-48 (Updated 5/21/08 effectively)

System claims 28-48 disclose similar limitations as claims 1-21 and are rejected for the same reasons as claims 1-21 respectively.

Regarding Claim 50, 52-54

System claims 50 & 52-54 disclose similar limitations as claims 23 & 25-27 and are rejected for the same reasons as claims 23 & 25-27 respectively.

Regarding Claim 55 (Updated 5/21/08 effectively)

System claim 55 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 56 & 57

System claims 56 & 57 disclose similar limitations as claims 16 & 17 and are rejected for the same reasons as claims 16 & 17 respectively.

Regarding Claim 58 (Updated 5/21/08 effectively)

Article of Manufacture (computer program) claim 58 discloses similar limitations as claim 1 and is rejected for the same reasons as claim 1.

Regarding Claims 59-61

Jain teaches use of Navier Stokes and other known simulation solutions (reuse) for solving various simulation problems as initial condition (Jain: Pg. 367-368 Section "Governing Rationale" Sub-Section A. Governing Equations). Sonderman also teaches initializing the models with input data (Sonderman: Col.7 Lines 8-20).

4. **Claims 22 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter), further in view of IEEE article "Heat Analysis on Insulated Metal Substrates" by Naomi Yunemura et al (Yunemura hereafter).**

Regarding Claim 22

Teachings of *Sonderman, Chen and Jain* are disclosed in claim 1 rejection above. Sonderman also teaches that the first principle simulation models the equipment conditions, thereby modeling temperature response and pressure response during various processes (Sonderman: at least in Col.5 Lines 62-67).

Sonderman, Chen and Jain does not teach explicitly that such temperature and pressure modeling is done using ANSYS computer code. *However, Jain teaches SIMD based processing to solve the computer-encoded differential equations (Jain: Pg. 370 Section III Parallel architectures for solving PDE).*

Yunemura teaches that heat simulation modeling can be performed using ANSYS computer code (Yunemura: Pg. 1407 Section 1) on a silicon chip.

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Yunemura to Sonderman, Chen and Jain to create a equipment model as disclosed by Sonderman. The motivation to combine would have been that Yunemura teaches heat modeling on a silicon chip affecting the thermal conductivity (Yunemura: Pg.1407 Section 2) based on various thicknesses and Sonderman is solving the same issue for the equipment model that for example model the equipment for depositing the various layers and affects on heat and pressure. ANSYS is known in art to be used as thermal & pressure modeling tool based on finite element analysis. Yunemura's teaching thereby facilitates computer-encoded differential equations solving which is

considered to be prime issue by Jain (Jain: See Section III, Networking and Dedicated MPE's for solving the computer-encoded differential equations).

Regarding Claim 49

System claim 49 discloses similar limitations as claim 22 and is rejected for the same reasons as claim 22.

5. **Claims 24 & 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of U.S. Patent No. 5,719,796 issued to Vincent M.C. Chen (Chen hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter), further in view of U.S. Patent No. 6,812,045 issued to Mehrdad Nikoonahad (Nikoonahad hereafter).**

Regarding Claim 24

Teachings of *Sonderman, Chen and Jain* are disclosed in claim 1 rejection above. Sonderman provides examples of the processing tool as etch and photolithography tools (Col.4 Lines 26-31) *but does not explicitly disclose chemical vapor and physical vapor deposition system.* Chen teaches fabrication equipment as Chemical Vapor Deposition (CVD) system (Col.5 Lines 1-5) but does not teach physical vapor deposition system. *Jain is moot on such teachings.*

Nikoonahad teaches deposition tools to include chemical vapor and physical vapor deposition system (Nikoonahad: Col.24 Lines 3-49).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Nikoonahad to *Sonderman, Chen and Jain*. The motivation to combine would have been that Nikoonahad and Sonderman-Chen are analogous art and both are modeling the semiconductor processing and providing feedback to the semiconductor processing tool (Sonderman: Abstract; Nikoonahad: Col.3; Col.93 Lines 20-35; Chen:Summary).

Regarding Claim 51

System claim 51 discloses similar limitations as claim 24 and is rejected for the same reasons as claim 24.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AKASH SAXENA whose telephone number is (571)272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Akash Saxena/
Examiner, Art Unit 2128